SYSTEM AND METHOD FOR REDUCING TIMING VIOLATIONS DUE TO CROSSTALK IN AN INTEGRATED CIRCUIT DESIGN

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ABSTRACT OF THE DISCLOSURE

[0054] A method involves: detecting a timing violation in a timing path included in an integrated circuit design; removing a wire, which couples two nodes in the integrated circuit design and is included in the timing path; and routing a new wire between the two nodes. The new wire is longer than the removed wire. The method can also involve: calculating timing information (e.g., delay and/or slew information) for the wires included in the timing path and selecting the wire for removal dependent on the timing information. In some embodiments, such a method eliminates timing violations that arise due to crosstalk in a single post-timing-analysis routing pass.